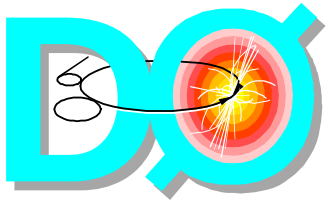


The DØ Run 2b Level 2 Trigger Upgrade

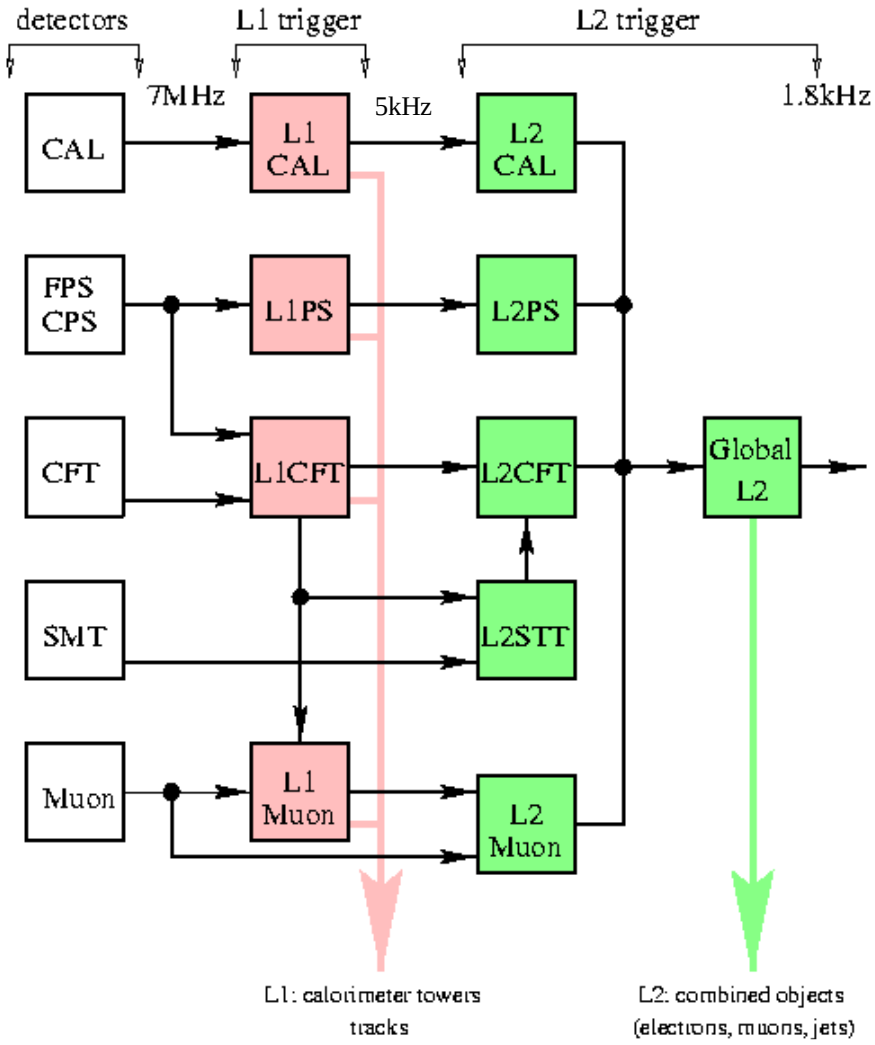
James Linnemann, Michigan State University,
for the DØ collaboration

Fermilab Director's Review

December 3, 2001

DØ Trigger Architecture

- Level 1
  - Calorimeter trigger
  - Fiber tracker trigger
  - Preshower (e/γ) trigger
  - Muon trigger
- Level 2
  - Silicon track trigger
  - Introduce Correlations, Refine Level 1 decision
- Level 3
  - Full event information available
  - Farm of high-performance computing nodes



Run 2b L2 Upgrade Goals

- Critical need to upgrade trigger systems
  - Increase trigger rejection to maintain existing rates with higher luminosity
  - Ensure efficient triggering for full range of Higgs channels
- The challenge for Level 2
  - **Input rate to Level 2 limited to ~ 5 kHz (readout time)**
  - **Output to Level 3 limited to 1.8kHz by calorimeter readout**
  - Need to get the events to level 3, where more handles are available
  - Need for higher L1 rejection: **moved L2 algorithms to L1**

How to maintain rejection in L2?

Do more processing in L2!

- **Before L=5x10^{32} cm^{-1}s^{-1}**
  - **Beta processors to replace Alpha processors**
- **Prepare L=5x10^{32} cm^{-1}s^{-1}**
  - **Upgrade L2STT** processor to take advantage of improved SMT
  - Upgrade L2 Processors with **Faster Beta processors**

Why Beta Processors?

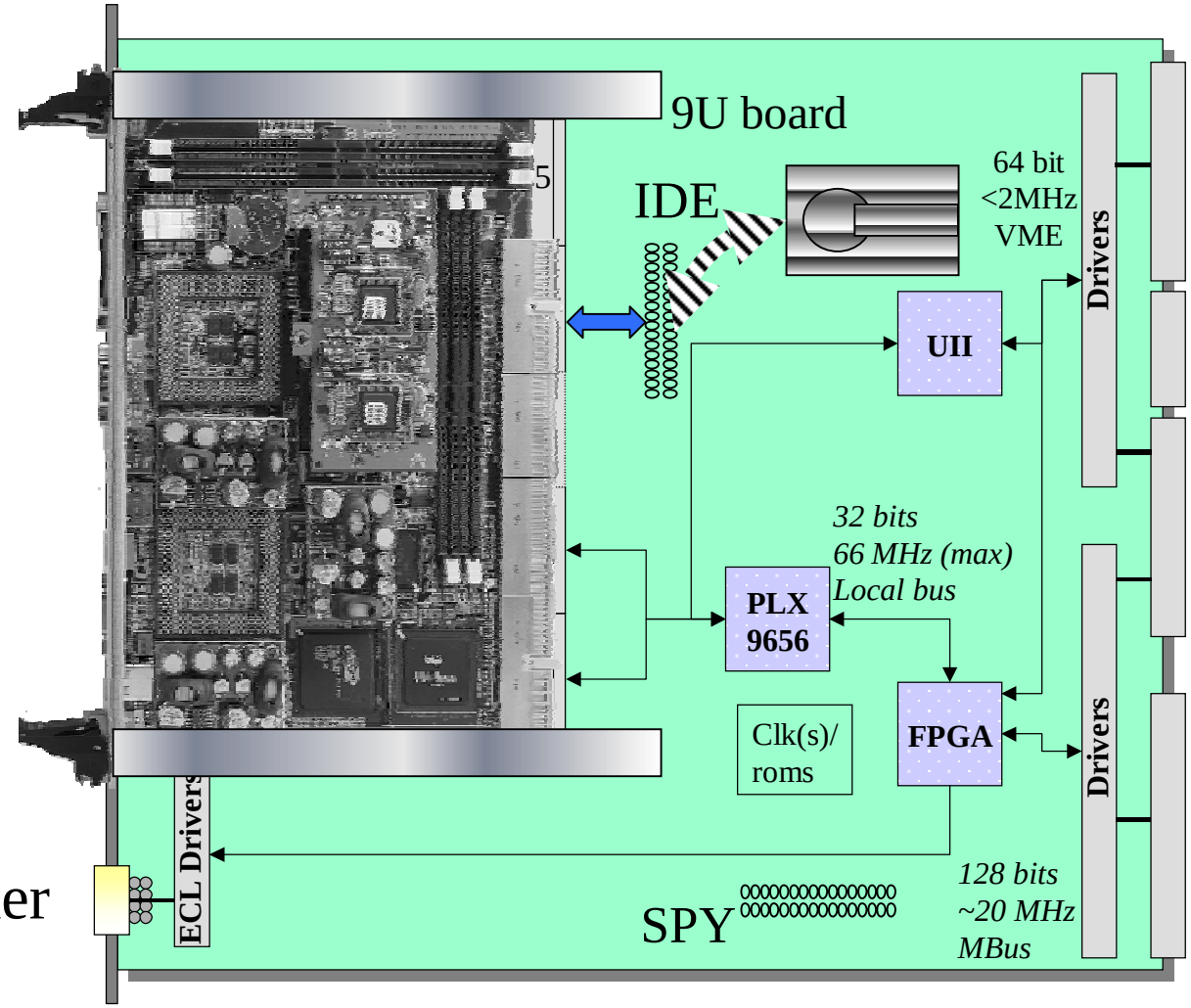
- Motivation: low yield of Alpha processors
  - Only **15**/38 worked
    - Mainly **fabrication problems** vias; BGA handling
    - Obsolete parts: no chance for extra production run
  - **Need** 16+8+2=**26** (system + test stand + spares) for baseline system
    - Need **test stand to avoid deadtime** for algorithm testing
- Replace all Alphas with Betas
  - Commission with Alphas
    - No change in high-level code to run on Betas, but 2-3 times faster
  - Confine software changes for maximum performance to one flavor
    - Simpler software: advantage of raw processor speed
    - Pentium Linux support much better
      - If needed, interrupt routine much easier in Pentium
- Phased Introduction of Betas
  - 38 production motherboards in 2002
    - Designed to allow processor upgrades
  - 26 processors in summer 2002
  - 12 **additional (faster) processors:** **Upgrade** for 2003/4

L2βeta: 850MHz CPU; 64b 66MHz PCI

- PIII Compact PCI card
- 9U card with custom devices

3 BGA's:

- Universe II **VME** interface
- PLX 64-bit **PCI** interface chip
- **MBus** and other logic in **FPGA**



L2βeta hardware advantages

- Alpha is frozen in CPU power
  - No upgrade path
- Beta benefits from Moore's Law in cPCI marketplace
  - × 2-3 CPU speedup over alpha gains 1.5-2 in throughput
    - Can use tradeoff to simplify online software
    - More gain with more sophisticated software
      - hide fixed overheads by overlapping operations
- Will build all Beta motherboards
  - Maximum flexibility in adding CPU's (more betas than baseline)
    - Could add 12 CPU's rather than just replacing 12
  - Incremental cost for 38 instead of 30 is only 20-30K (5%)

New/Improved features of L2β

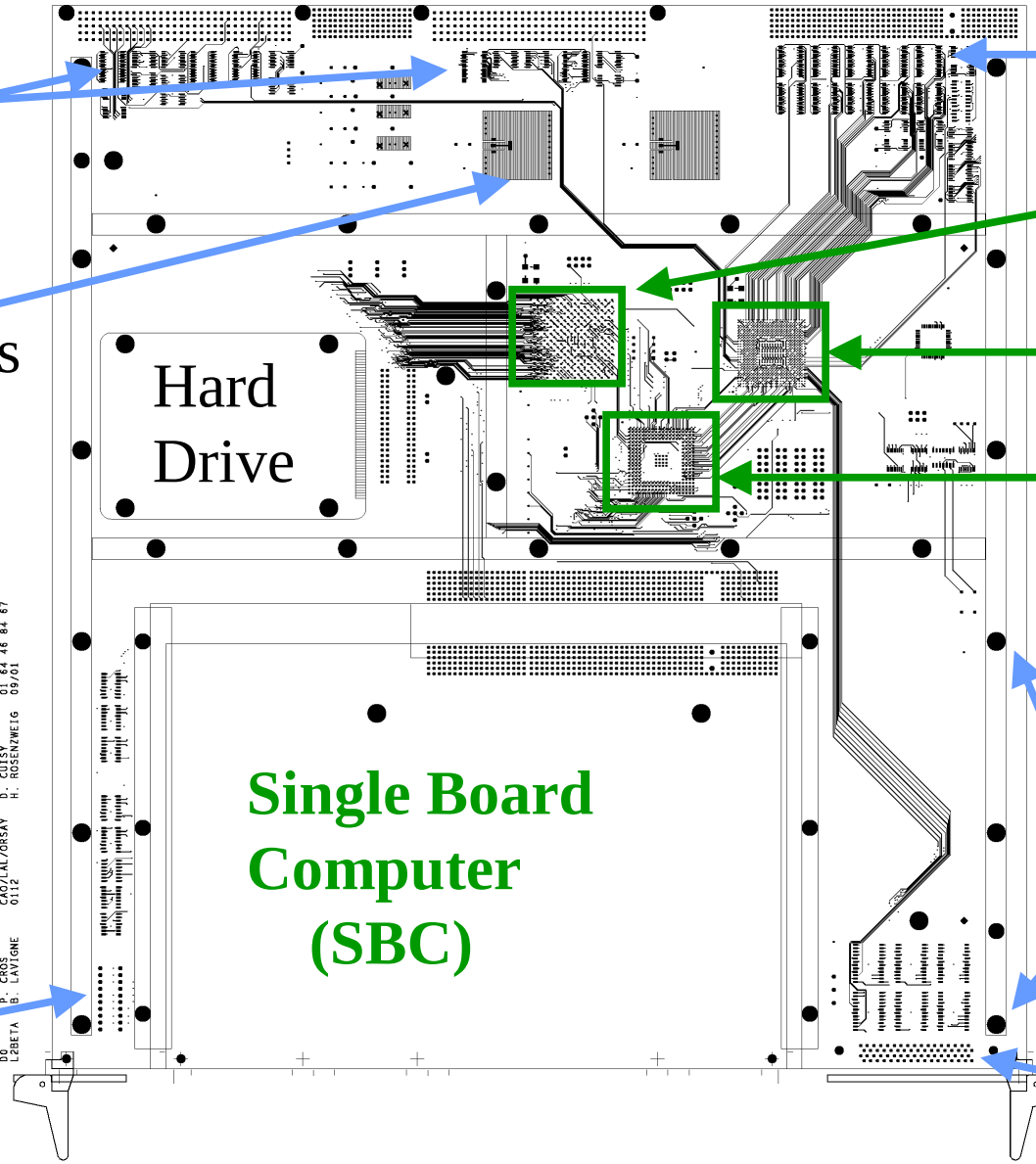
- ✓ ×3 CPU performance
- ✓ ×2 on-chip cache
- ✓ **Designed for Testing**
  JTAG, done by assembler
- ✓ More I/O pins
- ✓ More control in interrupt/resets

I/O Performance	
Alpha	~100 MB/s
MBT	~160 MB/s
L2βeta	~200 MB/s
SBC	~500 MB/s

CPU/MHz	Specint95	Specfp95
Alpha/500	~15	~21
PIII/850	~41	~35

Cheap upgrade:
add 2nd CPU
(but: write new software to use)

Level 2 βeta Board Layout



VME Drivers

Voltage converters

LEDs

MBus Drivers

VME Interface

FPGA (MBus)

PCI Interface

Mounting holes
For rails/stiffeners

ECL out

Level 2 Silicon Track Trigger

- Vital for triggering on b-quarks

  $ZH \rightarrow \nu\nu bb$

  $Z \rightarrow bb$ (top mass jet energy scale)

- Goal: 98% efficiency for tracks with

  $P_T > 1.5$ GeV

  Impact parameter < 2mm

- L2STT 2a installation Summer 2002

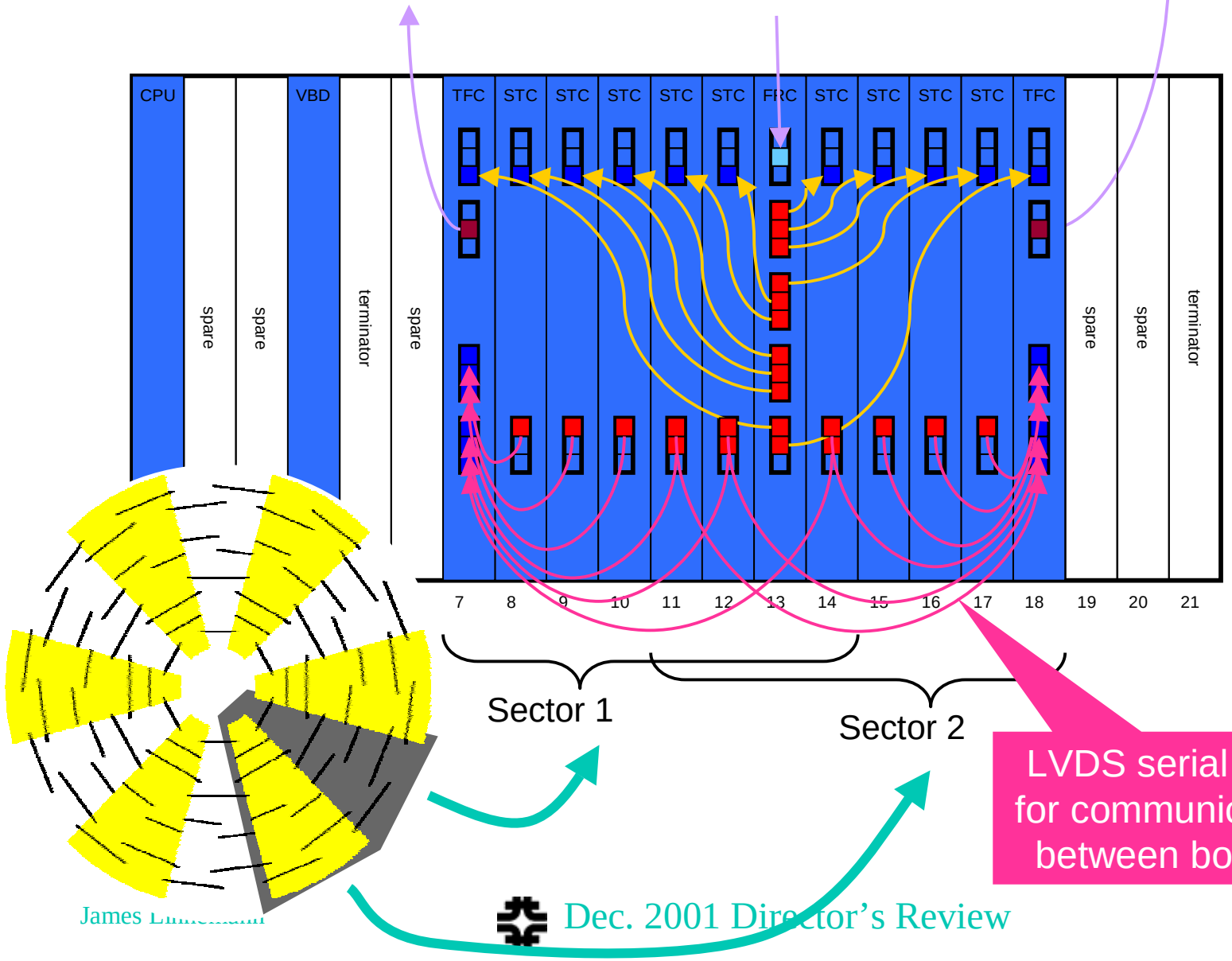
  1.8M NSF/DOE MRI funding (beyond 2a baseline)

- **Upgrade** to accommodate design of new silicon detector

- Most efficient:

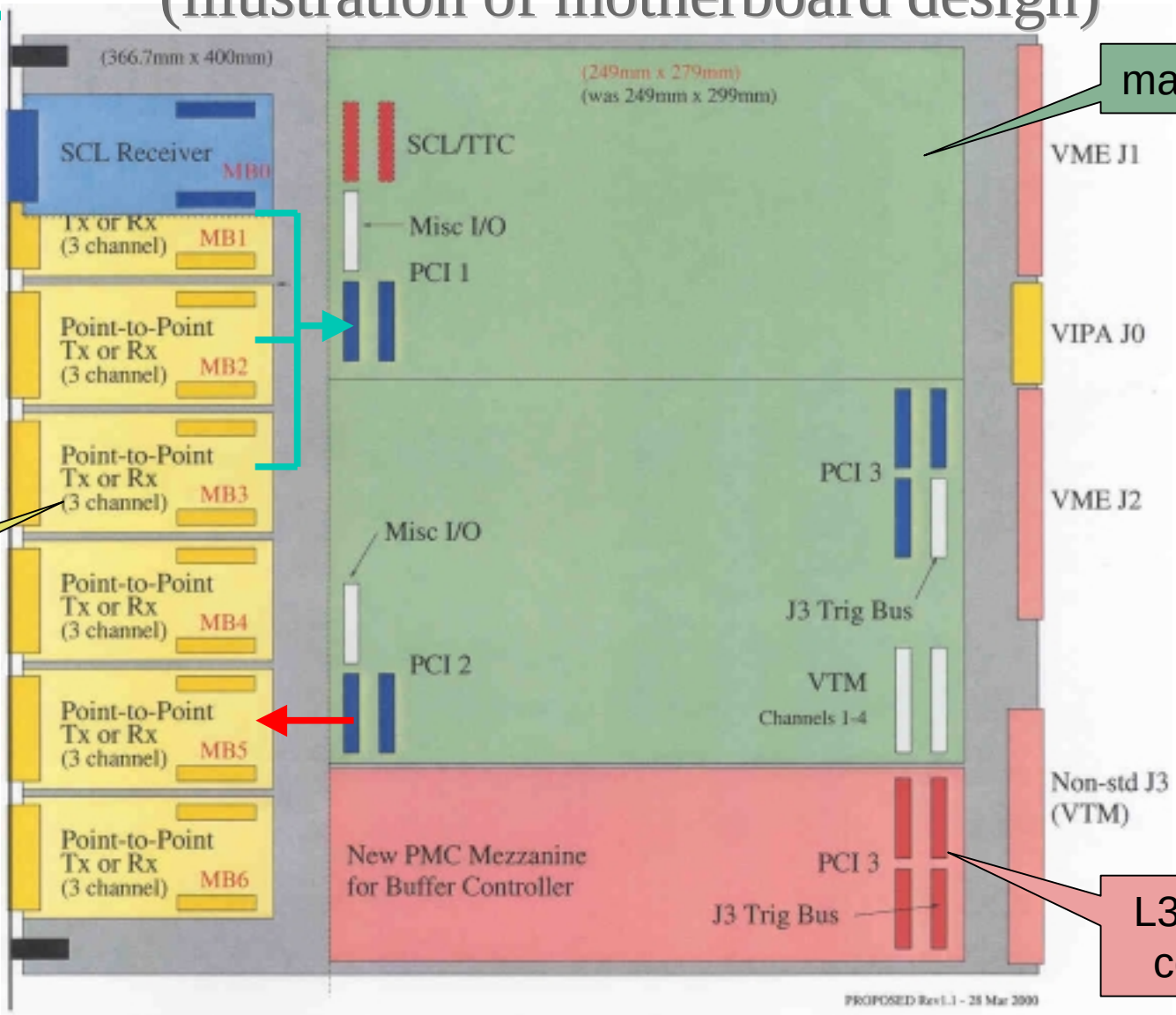
  build additional modules in early '02 production

L2STT Crate


CPU
spare
spare
VBD
terminator
spare
TFC
STC
STC
STC
STC
STC
FRC
STC
STC
STC
STC
TFC
spare
spare
terminator
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
Sector 1
Sector 2
LVDS serial links for communication between boards

Track Fit Card

(illustration of motherboard design)



max 9 LVDS in
(1 from FRC
8 from STC)

link rx

main logic

L3 buffer control

Card Flavors Glossary

- Fiber Road Card
  - receive SCL
  - fan out L1CTT data
  - manage L3 buffers
  - arbitrate VME bus
- Silicon Trigger Card
  - preprocess SMT data
    - cluster into hits
  - associate hits with CFT tracks
- Track Fit Card
  - fit trajectory to hits
- CPU (commercial)
  - initialization
  - downloading
  - monitoring
  - resets
- VME Buffer Driver
  - Readout to L3
  - Same as all other crates in DØ

STT Status

- Fiber Road Card being tested with real inputs at DØ
- STC (silicon hit clusters in track roads)
  - Prototype I currently being tested
  - Second prototype being debugged
- Track Fit Card tested at Stony Brook
  - Processed events with multiple track input roads
  - Running with DSP fitting code
- Buffer Controller sub-card being tested

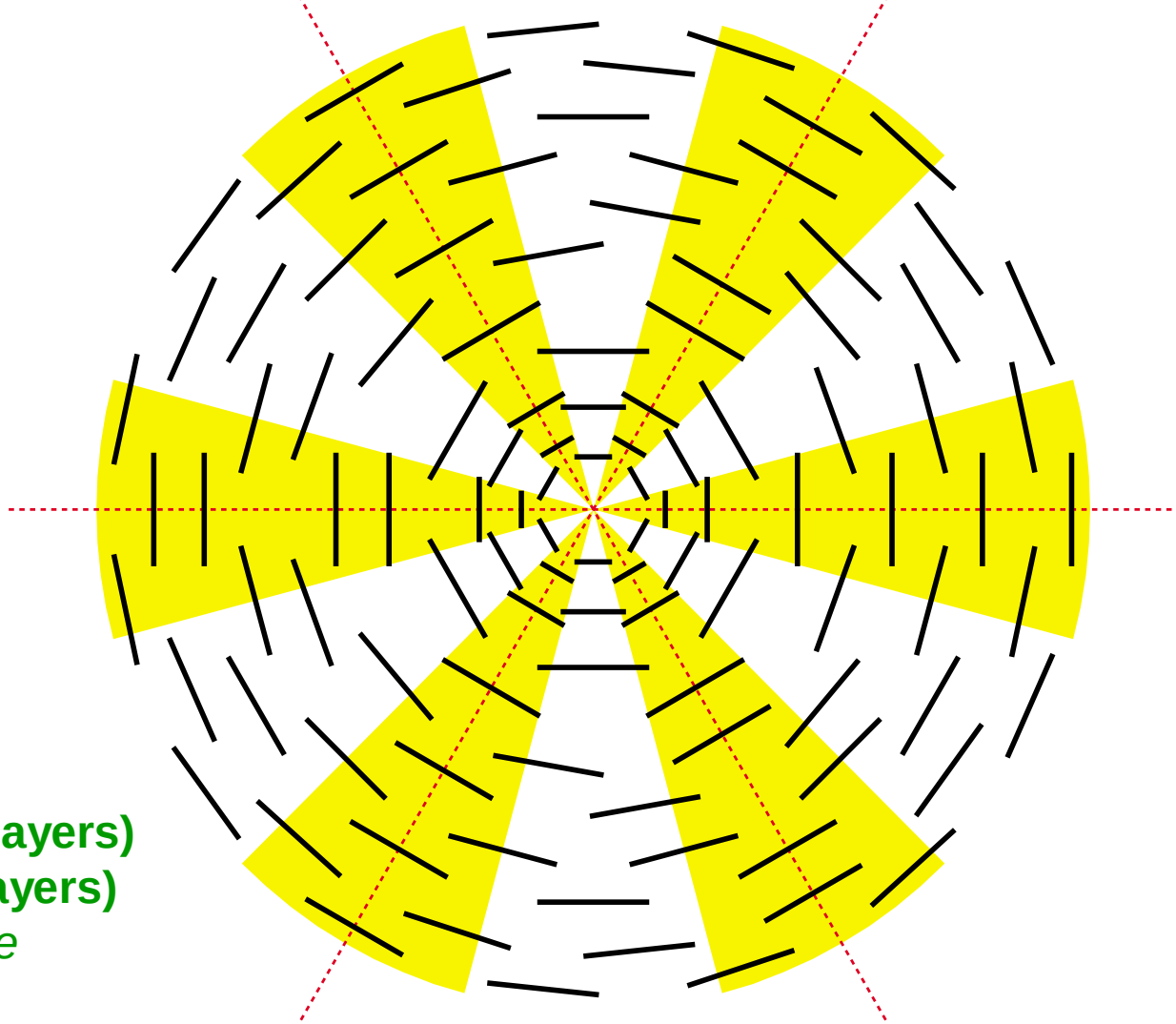
Link Transmitter

Motherboard, transmitters, receivers used by all boards

STC Prototype I

STT Upgrade: use all 6 SMT layers

Layer	2a	2b
0		2
1	3	3.5
2	5	6.1
3	7	9.5
4	9.5	12.7
5		15.5



Reuse Run 2a STT (4 layers)
Add 18 STC (2 new layers)
1 layer = full ϕ coverage
visually: 2 "layers"

L2STT Upgrade Staging

- Baseline: upgrade to use all **6 layers** from new SMT
  - Add more Silicon Track Cards (STC)
    - Revise firmware and software to support new detector configuration
    - Add matching I/O cards to handle extra signals
    - Add extra track fit cards
  - Requires a new fanout card and replacing backplanes
  - **Funding profile: can't build cards during 2002 STT production run**
- Staging: instrument **5 layers** first
    - Relatively inexpensive
    - Try to build boards from Run2a STT MRI contingency
  - Fewer STC and I/O cards needed
  - No new backplane or fanout card needed
  - Still need firmware and software updates
  - MC studies to study impact

Level 2 Cost Summary

L2 Betas	Estimate	+ contingency
Engineering *(contributed in-kind)*	166K	
Prototypes + Boards (38 @ 2.4K)	147K	
Single Board Computers (30 @ 4.3K)	130K	
Total L2 Betas (Alpha Replacement)	443K	596K (+35%)
Engineering	20K	
Single Board Computers (12 @ 4.3K)	52K	
Total L2 Beta Upgrade Processors	72K	98K (+37%)

L2STT Stage I	Estimate	+ contingency	L2STT Upgrade	Estimate	+ contingency
6 STC	41K		20 STC 8 TFC 20 VTM	286K	
STC Firmware	34K		STC Firmware	34K	
Cabling	6K		Cabling	19K	
			Echo Board, Backplane	63K	
Stage I (5 layers)	81K	129K (+59%)	**Baseline STT (6 layers)**	402K	593K (+48%)

L2 Schedule: Some Highlights

L2 Beta (Alpha Replacement)		
Layout	Done (except holes for rails)	
Prototypes (w/ Firmware)	**February 2002**	*fully funded*
Production, Installation	July-December 2002	
L2 Beta Upgrade		
Prototype Processor	April-October 2003	
Buy, Assemble and Install	October 2003 - March 2004	
Run 2a STT		
Production Start	**January 2002**	*fully funded*
Commissioning	July 2002	
Run 2b STT		
Stage 1 Parts Acquisition	December 2001	*funded*
Echo Board, Cables, etc.	Start June 2002	*9-21 mo. slack*
Software, Firmware start	Start January 2003	*12 mo. slack*
Test, Commission	July-Sept 2004	

Conclusions

- **L2 Betas** replacing Alpha Processors for Level 2 Processors
  - Prototypes being built to replace Alphas now
  - Add upgraded commercial processors for Run 2b
- **L2STT Staged Upgrade** to utilize Run 2b Silicon Tracker
  - Reuse all boards from Run 2a STT
    - Upgrade firmware, software
  - 5 layers first (relatively small increment)
  - Full 6 layers installation limited by funding profile